Abstract of the Disclosure

In some embodiments, a chip includes first and second ports to provide first and second received data signals and first and second received strobe signal, respectively. An internal clock signal has a fixed phase relationship to the first received strobe signal and the second received strobe signal has an arbitrary phase relationship with the internal clock signal. First and second write blocks latch the first and second received data signals synchronously with the first and second received strobe signals, respectively. Other embodiments are described and claimed.

P:/P17780/P17780APP.DOC 12/30/03